REMARKS

Claims 1-9 are rejected under 35 USC 103a as being unpatentable over Fujii et al. US Patent No: 5,898,695 [herein after Fujii] and further in view of Ling et al, US Patent No: 6,732,255 [herein after Ling]

Applicant asserts that claim 1 should not be rejected as being unpatentable over Fujii and further in view of Ling because neither Fujii nor Ling teach "when being informed by the host chip, the slave chip starting to transmit the data to the host chip", as is claimed in claim 1 of the present invention. The Examiner stated in the Office action mailed 08/24/2006 that said limitation is taught in Col 6, Lines 55-60, and quoted the text "...and data is written in RAM without passing through the register of the microprocessor." Applicant points out that the Examiner has interpreted the microprocessor 12 to be the host, however, the quotation chosen by the Examiner to support the above limitation directly conflicts with the limitation. That is, the data is not transmitted to the host chip. Instead, Fujii teaches (as the Examiner quoted) that the data is written in RAM 7 (shown in Fig.2 - not a part of the microprocessor 12) without passing through the register of the microprocessor. (emphasis added) For at least the reasons that writing data into RAM 7 without passing through the register of the microprocessor is not equivalent to "when being informed by the host chip, the slave chip starting to transmit the data to the host chip", as is claimed in claim 1, applicant asserts that claim 1 should not be found rejected as being unpatentable over Fujii and further in view of Ling. Reconsideration of claim 1 is respectfully requested. As claims 2-20 are dependent upon claim 1, if claim 1 is found allowable, so too should claims 2-20. Reconsideration of claims 1-20 is respectfully requested. Further comments regarding the patentability of particular dependent claims is provided below.

In the rejection of original claim 2 by the Examiner in the Office action mailed 08/24/2006, the Examiner stated that the limitation "wherein the host chip further delivers a clock signal to the slave chip" is taught by Fujii in Fig.5, element 4. However, inspection of Fig.5 shows that the micro-processor 12 (interpreted by the Examiner as the host) does not

deliver a clock signal to the transfer buffer 141 (interpreted by the Examiner as the slave). In particular, clock generator 4 does not generate a clock signal that is delivered to the slave chip. Instead, the clock generator 4 is shown generating a clock signal that is delivered to the microprocessor 12, which was interpreted as the host by the Examiner.

Further analysis of Fig.5 shows there are in fact two clock signals taught by Fujii and shown in Fig.5 that are delivered to the transfer buffer 141; however, applicant points out that neither is delivered by the microprocessor 12. Col 6, lines 49-54 only state, "The transfer buffer 141 is a buffer for outputting a TS packet onto a data bus, and transfers the data at high speed to RAM 7 through direct memory access (DNA), by performing data bit conversion and time axis conversion from transport path clock tsClock into data bus clock busClock." Applicant notes that the transport path clock is delivered by the transport path, and Fujii does not teach from where the busClock is delivered. Therefore, applicant asserts that claim 2 should not be found as being unpatentable over Fujii and further in view of Ling for at least the reason that neither reference teaches the host chip is for delivering a clock signal to the slave chip.

New Claims

Applicant has added new dependent claims 10-20. No new matter is entered.

Concerning claim 10, paragraph [0004] of the present invention states, "Normally, the host chip is a digital chip, and the slave chip is an analog chip." Applicant points out that neither Fujii nor Ling teach such a configuration.

Concerning claim 11, paragraph [0023] of the present invention states, "Take an optical disk drive for example." Applicant points out that neither Fujii nor Ling teach the multi-chip system being an optical disk drive.

Concerning claim 12, paragraph [0005] of the present invention states, "A mutli-chip system normally includes at least a host chip engaged in controlling the operation of the system, and at least a slave chip engaged in executing servo control or detecting some particular signals." Also refer to paragraph [0005] stating, "The task of the slave chip is to

execute the servo control of the optical disk drive". Applicant points out that neither Fujii nor Ling teach the slave being a servo control chip and the host being for controlling operations of the optical disk drive.

Concerning claim 13, Fig.3 of the present invention shows that the clock cycles on the clock pin pair are not delivered to the slave chip until after the request pin pair is informed by the slave chip. Also, paragraph [0022] of the present invention states, "When the host chip 110 detects the voltage change of the request pin pair 130, the host chip 110 starts to deliver a clock signal via the clock pin pair 160 to the slave chip 120". Applicant points out that neither Fujii nor Ling teach the host chip not delivering the clock signal to the slave chip when not being informed by the slave chip.

Concerning claim 14, paragraph [0022] of the present invention states, "The host chip 110 and the slave chip 120 implement data transmission within these thirteen clock cycles." Applicant points out that neither Fujii nor Ling teach the clock signal having a predetermined number of clock cycles. Applicant also notes that continuous clock cycles generated by the clock generator 4 should not be interpreted as a predetermined number of clock cycles because continuous clock cycles is not equivalent to a predetermined number of clock cycles.

Concerning claims 15-21, as illustrated in Fig.3, paragraph [0023] of the present invention states, 'If the data to be transmitted in the first, second, third, fourth, fifth, and sixth clock cycles are respectively the tracking servo signal, focusing servo signal, tray open signal, tray close signal, disc blank signal, and disc defect signal, the host chip 110 can then obtain the following information: the state of the tracking servo signal is "1", the state of the focusing signal is "1", the state of the tray open signal is "1", the state of the tray close signal is "0", the state of the disc blank signal is "0", and the state of the disc defect signal is "1".' Applicant points out that neither Fujii nor Ling teach said servo signals, one servo signal being transmitted by the slave chip to the host chip during each clock cycle.

Sincerely yours,

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